Listing of the Claims:

Note: No claims have been amended, and the following listing of claims is provided for reference only.

1 (original): A method of data coding/decoding, the method comprising:

reading a data matrix, the data matrix comprising a plurality of data elements;

constructing a reference matrix based on the data matrix so that the reference matrix comprises a plurality of reference elements each corresponding to a data element, each reference element representing whether its corresponding data element fits a default or not; and

taking a decision step for each data element when the data matrix is written into a memory so that when a reference element corresponding to a data element represents that the data element fits the default, the data element is prevented from being written into the memory.

2 (original): The data coding/decoding method of claim 1 further comprising:

in the decision step, wherein when a reference element corresponding to a data element represents that the data element does not fit the default, the data element is written into the memory.

3 (original): The data coding/decoding method of claim 1 further comprising:

receiving an image data;

generating a block based on the image data;

taking a frequency-domain transformation to the block for generating an output data; and

generating the data matrix based on the output data.

4 (original): The data coding/decoding method of claim 3 wherein the frequency-domain transformation is a two-dimensional discrete cosine transformation.

5 (original): The data coding/decoding method of claim 3 wherein when output data based on the frequency domain transformation generates the data matrix, the data matrix is generated by quantizing the output data.

6 (original): The data coding/decoding method of claim 1 further comprising:

taking a second decision step for each reference element when a data matrix stored in the memory is read so that the memory is prevented from being read when a reference element corresponding to a data element represents that the data element fits the default.

7 (original): The data coding/decoding method of claim 6 further comprising:

in the second decision step, wherein if a reference element corresponding to a data element represents that the data element does not fit the default, the data element is read from the memory.

8 (original): The data coding/decoding method of claim 6 further comprising:

after a reference element undergoes the second decision step, each reference element not yet undergoing the second decision step undergoes a checking step for checking if there is another reference element representing that its corresponding data element does not fit the default.

9 (original): The data coding/decoding method of claim 8 further comprising:

in the checking step, if all reference elements not yet undergoing the second decision step represent that their corresponding data elements fit the default, reading of the data matrix is stopped.

10 (original): The data coding/decoding method of claim 1 wherein each reference element is a one-bit data for representing whether its corresponding data fits the default or not.

11 (original): The data coding/decoding method of claim 1 wherein the default is null.

12 (original): A data coding/decoding method comprising:

reading a reference matrix before reading a data matrix from a memory, wherein the reference matrix comprises a plurality of reference elements each corresponding to a data element of the data matrix, each reference element representing whether its corresponding data element fits a default or not; and

taking a decision step for each reference element of the reference matrix when the data matrix is read from the memory so that the memory is prevented from being read when a reference element corresponding to a data element represents that the data element fits the default.

13 (original): The data coding/decoding method of claim 12 further comprising:

in the decision step, when a reference element corresponding to a data element represents that the data element does not fit the default, the data element is read from the memory.

14 (original): The data coding/decoding method of claim 12 further comprising:

after each reference element undergoes the decision step, a checking step is taken for each reference element not yet undergoing the decision step for checking if there is another reference element representing that its corresponding data element does not fit the default.

15 (original): The data coding/decoding method of claim 14 further comprising:

in the checking step, wherein if any reference element corresponding to a data element not yet undergoing the decision step represents that the data element fits the default, reading of the data matrix is stopped.

16 (original): A processing circuit for data coding/decoding comprising:

a memory capable of storing a data matrix wherein the data matrix comprises a plurality of data elements;

a register module for storing a reference matrix wherein the reference matrix comprises a plurality of reference elements each corresponding to a data element, each reference element for representing whether its corresponding data element fits a default or not; and

a decision module, wherein when the data matrix is written into the memory by the processing circuit, the decision module is capable of checking each data element so that when a reference element corresponding to a data element represents that the data element fits the default, the data element is prevented from being written into the memory.

17 (original): The processing circuit of claim 16 wherein when the decision module takes a decision, the data element is written into the memory if the reference element corresponding to a data element represents that the data element does not fit the default.

18 (original): The processing circuit of claim 16 further comprising:

a frequency-domain transformation module for processing a frequency-domain transformation to a block for generating an output data; and

a quantization module for generating the data matrix based on the output data.

19 (original): The processing circuit of claim 18 wherein the frequency-domain transformation is a two-dimensional discrete cosine transformation.

20 (original): The processing circuit of claim 18 wherein the quantization module generates the data matrix by quantizing the output data.

21 (original): The processing circuit of claim 16 wherein when the processing circuit reads a data matrix stored in the memory, the decision module is capable of

taking a further decision for each reference element so that when a reference element corresponding to a data element represents that the data element fits the default, the processing circuit is prevented from reading the data element from the memory.

22 (original): The processing circuit of claim 21 wherein when the processing circuit reads a data matrix stored in the memory, the data element is permitted to be read from the memory by the decision module if the reference element corresponding to a data element represents that the data element does not fit the default.

23 (original): The processing circuit of claim 21 further comprising:

a checking module, wherein after the decision module processes decisions for each reference element, the checking module is capable of processing a further checking step for each reference element without taking the further decision for checking if there is another reference element representing that its corresponding data element does not fit the default.

24 (original): The processing circuit of claim 23 wherein after the checking module proceeds with checks, the processing circuit reading the data matrix is stopped by the checking module if all reference elements not undergoing the decision represent that their corresponding data elements fit the default.

25 (original): The processing circuit of claim 16 wherein the default is null.

26 (original): The processing circuit of claim 16 wherein the register module is a shift keying register, and each reference element is a one-bit data for representing whether its corresponding data element fits the default or not.

27 (original): The processing circuit of claim 26 further comprising:

a shift keying control module, wherein when the processing circuit reads the data

element from the data matrix by a default sequence, the shift keying control module controls shift keying of the register module sequentially by the default sequence so that the decision module is capable of checking each reference element corresponding to each data element sequentially.

28 (original): A processing circuit for data coding/decoding comprising:

a memory for storing a data matrix wherein the data matrix comprises a plurality of data elements;

a register module for storing a reference matrix, the reference matrix comprising a plurality of reference elements each corresponding to a data element, each reference element for representing whether its corresponding data element fits a default or not; and

a decision module, wherein when the data matrix is written into the memory by the processing circuit, the decision module is capable of processing a checking step based on each reference element of the reference matrix so that when a reference element corresponding to a data element represents that the data element fits the default, the data element is not written into the memory.

29 (original): The processing circuit of claim 28 wherein when the decision module processes a decision, the data element is written into the memory if the reference element corresponding to a data element represents that the data element does not fit the default.

30 (original): The processing circuit of claim 28 further comprising:

a checking module, wherein after the decision module processes decisions for each reference element, the checking module is capable of processing a further checking step for each reference element not yet undergoing the decision of the decision module for checking if there is another reference element representing that its corresponding data element does not fit the default.

31 (original): The processing circuit of claim 30 wherein after the checking module processes checks, the processing circuit reading the data matrix is stopped by the checking module if all reference elements not yet undergoing the decision represent that their corresponding data elements fit the default.

32 (original): The processing circuit of claim 28 further comprising:

a shift keying control module, wherein when the processing circuit reads the data element of the data matrix by a default sequence, the shift keying control module controls shift keying of the register module sequentially by the default sequence so that the decision module is capable of checking each reference element corresponding to each data element sequentially.

33 (original): A data coding/decoding method comprising:

reading a frequency-domain matrix, the frequency-domain matrix comprising a plurality of frequency-domain elements;

providing a reference matrix comprising a plurality of reference elements each corresponding to a frequency-domain element, each reference element representing whether its corresponding frequency-domain element fits a default or not; and

taking a transformation step for generating an output matrix based on the frequency-domain matrix, the transformation step comprising:

taking a transformation checking step for checking if the reference matrix fits a default matrix; if the reference matrix does not fit the default matrix, a corresponding output matrix is generated by proceeding to a transformation operation for the frequency-domain matrix; and

if the reference matrix fits the default matrix, the frequency-domain matrix is prevented from undergoing the transformation operation and the output matrix is a constant matrix.

34 (original): The data coding/decoding method of claim 33 wherein at least one

frequency-domain element is a direct current frequency-domain element and other frequency elements are alternating current frequency-domain elements among the plurality of frequency-domain elements; wherein when the reference matrix fits the default matrix, each reference element corresponding to each alternating current frequency-domain element in the reference matrix represents that the alternating current frequency-domain element fits the default.

35 (original): The data coding/decoding method of claim 34 further comprising:

when the reference matrix fits the default matrix, a constant operation step is performed for generating the constant matrix by working out a constant value based on the direct current frequency-domain element so that a plurality of elements of the constant matrix equal the constant value.

36 (original): The data coding/decoding method of claim 33 wherein the default is null.

37 (original): The data coding/decoding method of claim 33 wherein the transformation operation is an inverse discrete cosine transformation.

38 (original): A processing circuit for data coding/decoding comprising:

a memory capable of storing a frequency-domain matrix, the frequency-domain matrix comprising a plurality of data elements;

a register module for storing a reference matrix wherein the reference matrix comprises a plurality of reference elements each corresponding to a frequency-domain element, each reference element for representing whether its corresponding frequency-domain element fits a default or not; and

a transformation module for providing a corresponding output matrix based on the frequency-domain matrix, the transformation module comprising:

a transformation operation module; and

a transformation checking module for checking if the reference matrix fits a

default matrix; wherein if the reference matrix does not fit the default matrix, the transformation checking module triggers the transformation operation module to proceed to a transformation operation for generating a corresponding output matrix, and if the reference matrix fits the default matrix, the transformation checking module is prevented from triggering the transformation operation module to proceed to the transformation operation for generating a corresponding output matrix and the output matrix is a constant matrix.

39 (original): A processing circuit for data coding/decoding of claim 38 wherein at least one frequency-domain element is a direct current frequency-domain element and other frequency elements are alternating current frequency-domain elements among the plurality of frequency-domain elements; wherein when the reference matrix fits the default matrix, each reference element corresponding to each alternating current frequency-domain element in the reference matrix represents that the alternating current frequency-domain element fits the default.

40 (original): The processing circuit for data coding/decoding of claim 39 further comprising:

a constant operation module; wherein when the reference matrix fits the default matrix, the transformation checking module triggers the constant operation module to generate a constant value and the constant matrix based on the direct current frequency-domain element so that a plurality of elements of the constant matrix equal the constant value.

41 (original): The processing circuit for data coding/decoding of claim 38 wherein the default is null.

42 (original): The processing circuit for data coding/decoding of claim 38 wherein the transformation operation module is capable of performing an inverse discrete

cosine transformation.